IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An electronic device comprising:

a data receiver having a trip point adjustor; and

a data corrector coupled to the data receiver ~~for~~ to adaptively ~~providing~~ provide trip point adjustment information to the trip point adjustor, the data corrector responsive to differential clock signals and a reference to generate the adjustment information.

2. (Currently Amended) ~~The electronic device of claim 1, further comprising~~ An electronic device comprising:

a data receiver having a trip point adjustor;

a data corrector coupled to the data receiver to adaptively provide trip point adjustment information to the trip point adjustor; and

a latch coupled between the data corrector and the data receiver ~~for~~ to conditionally ~~providing~~ provide trip point adjustment information to the trip point adjustor of the data receiver.

3. (Original) The electronic device of claim 1, wherein the trip point adjustment information comprises analog control voltages.

4.-6. (Cancelled)

7. (Currently Amended) An integrated circuit comprising:

a data receiver having a trip point adjustor; and

a data corrector coupled to the data receiver ~~for~~ to adaptively ~~providing~~ provide trip point adjustment signals to the trip point adjustor, the data corrector responsive to differential clock signals and a reference to generate the adjustment information.

8.-9. (Cancelled)

10. (Currently Amended) A memory device comprising:

a data receiver having a trip point adjustor; and

a data corrector coupled to the data receiver ~~for~~ to adaptively ~~providing~~ provide trip point adjustment information to the trip point adjustor of the data receiver, the data corrector responsive to differential clock signals and a reference to generate the adjustment information.

11. (Currently Amended) ~~The memory device of claim 10, further comprising~~ A memory device comprising:

a data receiver having a trip point adjustor;

a data corrector coupled to the data receiver to adaptively provide trip point adjustment information to the trip point adjustor of the data receiver; and

a latch coupled between the data corrector and the data receiver ~~for~~ to conditionally ~~providing~~ provide trip point adjustment information to the trip point adjustor of the data receiver.

12.-48. (Cancelled)

49. (Currently Amended) A processing system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of data receivers, each data receiver having a trip point adjustor; and

a data corrector coupled to each data receiver ~~for~~ to adaptively ~~providing~~ provide trip point adjustment information to the trip point adjustor of each data receiver, the data corrector responsive to differential clock signals and a reference to generate the adjustment information.

50-64. (Cancelled)

65. (New) The electronic device of claim 1, wherein the trip point adjustor includes a plurality of weighted p-type transistors and a plurality of weighted n-type transistors responsive to the adjustment information.

66. (New) The electronic device of claim 1, wherein the data corrector includes inputs to receive the differential clock signals as data signals.

67. (New) The electronic device of claim 1, wherein the data corrector includes a phase detector coupled to a filter, the phase detector and the filter to correlate differences between paired differential clock signals.

68. (New) The electronic device of claim 2, wherein the latch and the data corrector are configured to provide the adjustment information in a time period during which data is not transferred into or out of the data receiver.

69. (New) The electronic device of claim 2, wherein the latch is coupled to a plurality of data receivers to adaptively provide trip point adjustment information to each data receiver.

70. (New) The integrated circuit of claim 7, wherein the trip point adjustor includes a plurality of p-type transistors with different width to length ratios, the plurality of p-type transistors responsive to the adjustment information.

71. (New) The integrated circuit of claim 7, wherein the integrated circuit includes inputs to receive system clocks and a voltage reference to couple to the data corrector.

72. (New) The memory device of claim 10, wherein the memory is configured to receive a voltage reference external to the memory device as the reference.

73. (New) The memory device of claim 10, wherein the differential clock signals include free running clock signals.

74. (New) The memory device of claim 10, wherein the memory device includes a memory array to store data input to the data receiver.

75. (New) The memory device of claim 74, wherein the memory device includes a data latch interposed between the data receiver and the memory array.

76. (New) The memory device of claim 11, wherein the latch is configured to hold an eight bit adjustment vector.

77. (New) The memory device of claim 11, wherein the trip point adjustor has a trip point adjustment range of ± 200 millivolts.

78. (New) The processing system of claim 49, wherein the data corrector has inputs to receive external differential clock signals and an external voltage reference, wherein the data corrector is responsive to the external differential clock signals and the external voltage reference to generate the adjustment information.

79. (New) The processing system of claim 49, wherein the data corrector includes a phase detector coupled to a filter, the phase detector and the filter to correlate differences between paired differential clock signals.

80. (New) The processing system of claim 49, wherein the processing system includes a data bus to couple the processor to the memory device.

81. (New) The processing system of claim 49, wherein the differential clock signals include system clocks.